# ESDI Winchester Disk Controller

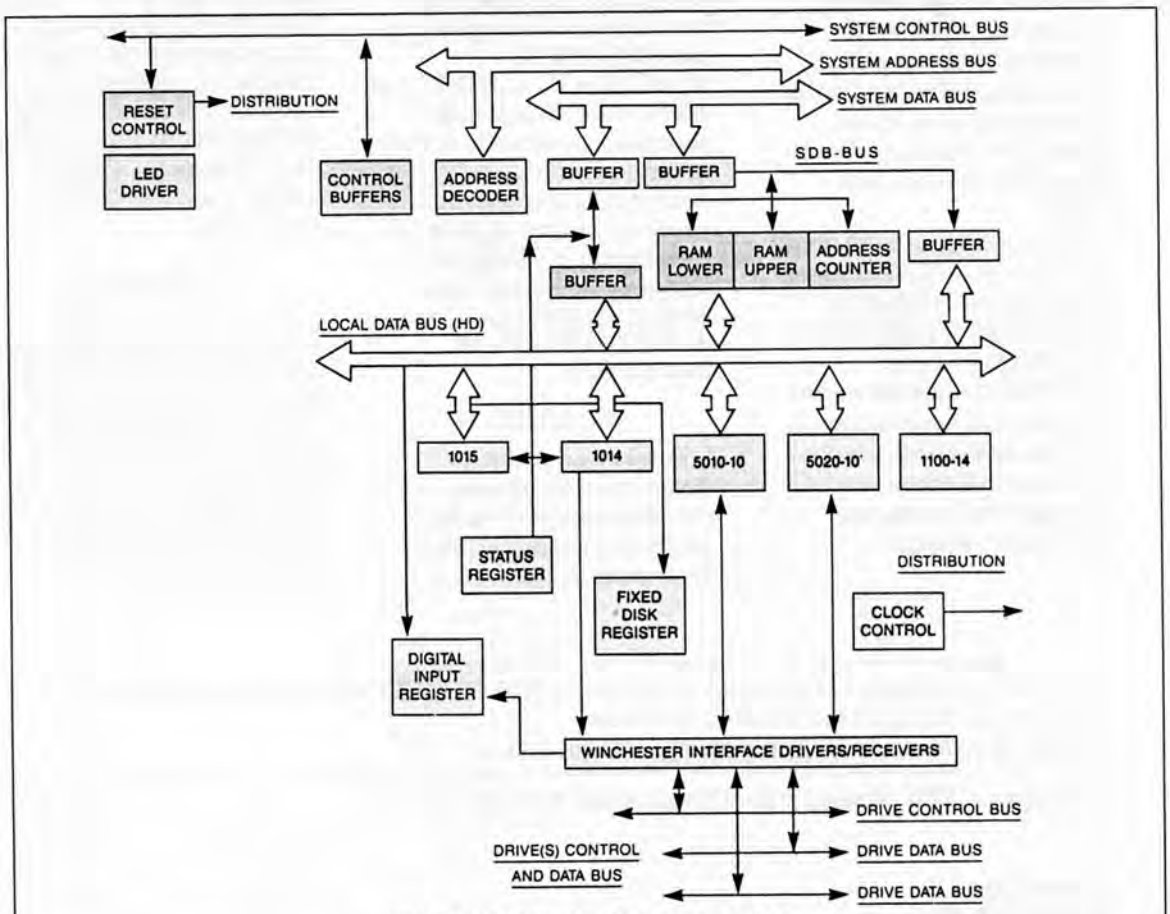
# WD1005-WAH

### Features

- ☐ PC XT height, full slot form factor
- ☐ AT bus compatible
- ☐ Controls one or two enhanced small device interface (ESDI) compatible drives with a maximum of 16 heads and 2048 cylinders
- ☐ MS-DOS mode translates logical tracks to physical tracks; i.e., 17 sectors per track to 34 sectors per track
- ☐ 16-bit data bus for high speed data transfers
- 8-bit, bi-directional bus for control and status transfers
- ☐ Multiple sector read/write commands (may cross head and cylinder boundaries)
- ☐ Read/write, diagnostic, and verify commands
- ☐ Implied and overlapped seek commands
- ☐ 56-bit ECC for Winchester error detection and correction
- ☐ Programmable retries/no retries
- ☐ Hard sectored format (512 bytes/sector, up to 36 sectors/track)
- ☐ Supports 3:1 interleave
- ☐ Two 2048 x 8 RAMs for sector data buffer
- ☐ Design based on a Western Digital chip set consisting of:
  - WD1014
  - WD1015-23
  - WD5010B-10
  - WD50C20A-10
  - WD1100-14

10.0 MBS data rate

Certifiable as a Class B Computing Device pursuant to Subpart J of Part 15 of F.C.C. Rules




WD1005-WAH BLOCK DIAGRAM

**WESTERN DIGITAL**

# ESDI Winchester Disk Controller

## Description

The WD1005-WAH Winchester Disk Controller is an IBM PC AT bus compatible module designed to interface one or two disk drives. The WD1005-WAH's drive interface conforms to the ESDI specification. Drives need not be of the same capacity or configuration. All necessary receivers and drivers are included on the board for direct connection to the drive(s).

Host System Address, Data, and Control Buses interface directly with the WD1005-WAH. Programmed Input/Output (PIO) is the only operational mode for all data, control, and status transfers. All data transfers, except ECC bytes during Read and Write Long operations, are sixteen bits wide. Control and status transfers are 8-bits wide.

Western Digital implements the WD1005-WAH's architecture with the WD10C14, WD1015-23, WD5010B-10, WD50C20A-10, and WD1100-14. Extensive error detection and correction, as well as data recovery techniques for disk errors, are incorporated within the controller's design.

## WD10C14

Module support registers within the WD10C14 include Command/Error, and Sector Size, Drive, Head (SDH) Registers. Only the WD1015-23 directly accesses the WD10C14's Command/Error Register. Either the host or the WD1015-23 may access the SDH Register.

## WD1015-23

This device is an 8-bit microprocessor that controls and coordinates the activity of the disk drives, WD5010B-10, WD50C20A-10, and WD1100-14. The WD1015-23 receives and sends command or status information over an internal multiplexed address/data bus. Access to the registers in the WD5010B-10, WD50C20A-10, or WD1100-14 aid the execution of host generated commands as well as error recovery procedures. Additionally, the WD1015-23 performs several module self-tests following a Diagnose Command. Firmware controlling these functions resides in the WD1015-23's 2K internal ROM.

## WD5010B-10

This advanced design VLSI device controls all data transfers between the Sector Buffer and the drives. The WD5010B-10 performs either single or multiple sector Read/Write commands. The WD5010B-10 also executes programmable format and error recovery algorithms. All commands are executed through the Task Files of the WD5010B-10 after limited intervention by the WD1015-23.

## WD50C20A-10

This companion chip to the WD5010B-10 converts the WD5010B-10 data format to the format required by ESDI drives. An 8-bit host interface data bus parallels the WD5010B-10 host interface data bus. Parallel buses transmit WD5010B-10 Task File information into the WD50C20A-10 Task File. A portion of the WD50C20A-10 Task File also stores ESDI information for serial data transfers in addition to device commands and status. The WD50C20A-10 in this application operates with hard sectored serial mode ESDI disk drives.

## WD1100-14

The WD1100-14 ECC polynomial generator/checker with a 12-bit correction span detects a single burst with up to 32 bits in error. Seven check/syndrome bytes (56 bits) are generated and appended to the data field for the error detection and correction process.

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