WD1007A-WAH/WA2 WINCHESTER/FLOPPY DISK CONTROLLER

FEATURES

- IBM* PC-AT* compatible Winchester and floppy disk controller
- ESDI Drive Interface
- Utilizes maximum storage capacity of ESDI drives
- Controls two fixed disk drives and two floppy disk drives (5.25 or 3.5 inch)
- 84-pin Buffer Management and Control (AMAC) gate array
- Optional BIOS ROM
- Supports 1:1 interleave
- Data transfer rate of 10 Mbits per second
- Supports NRZ disk data format
- Two 8192 x 8 RAMs for look-ahead read caching to reduce disk access time and increase data throughput
- Software selectable 56-bit ECC
- Multiple sector read/write commands

DESCRIPTION

The WD1007A-WA2 Winchester/Floppy Disk Controller (WFDC) module interfaces two ESDI-compatible fixed disk drives and two floppy disk drives (5.25 or 3.5 inch) to the PC-AT computer I/O Channel bus structure. An optional BIOS ROM provides parameter tables, low-level formatting and surface analysis routines to fully integrate ESDI drive capabilities into the system.

The fixed disk section of the module includes the WD50C12 Winchester Disk Controller, the WD1018 Buffer Manager/Control Processor, sector buffer RAM and associated control logic. The WD37C65A Floppy Disk Controller (FDC) implements the optional floppy disk control section. The WD12C00A (AMAC) gate array also provides buffering and control. The AMAC reduces module logic and supports a 1:1 interleave format.

A description of the functional blocks of the WD1007A-WA2 Winchester/Floppy Disk Controller (WFDC) appears below. Refer to the block diagram in Figure 1.

WD50C12 Winchester Disk Controller

The WD50C12 Winchester Disk Controller (WDC) is an advanced VLSI device that controls and coordinates the activity of the hard disk drive. The WDC supports 1:1 interleave and data transfer rates up to 10 Mbits per second. It utilizes the maximum storage capacity of ESDI drives by translating physical parameters into logical parameters for those operating systems which do not recognize more than 17 sectors per track or more than 1048 cylinders per drive. (See Translation in the Appendix for an explanation of this feature). The WDC offers software selectable 56-bit ECC and supports the NRZ data format.

WD1018 Buffer Manager/Control Processor

The WD1018 Buffer Manager/Control Processor is an eight-bit microcontroller that operates with the WD50C12 and the AMAC logic array to facilitate processing of disk commands. It provides sector data buffer management, helps in error recovery procedures and performs module diagnostics. The processor chip includes internal RAM and ROM memory.

WD12C00A-JU22 Logic Array (AMAC)

The primary function of the AMAC logic is to provide host address and command decoding, task file control and data buffering. The VLSI logic array replaces the standard WD1014 support device and several SSI/MSI components. This simplifies the logic and lowers power consumption. The AMAC logic includes the data and address registers, memory read/write control, and WD50C12 task file image registers. It interfaces to both the system and module (local) bus structures. (See Figure 2. AMAC Block Diagram)

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RAM Data Buffer

Two 8192 x 8 static RAM memories buffer the sector data between the drive(s) and the PC-AT system bus. They also buffer Error Correction Code (ECC) information between the WD50C12 disk controller and the WD1018 control processor. The sector buffers and the above control components provide a 1:1 sector interleave format for optimal system performance.

WD37C65A Floppy Disk Controller (FDC)

The optional WD37C65A Floppy Disk Controller (FDC) is a standard VLSI device that supports both single and double density diskette formats and provides data and control interfaces for the host and the floppy drive. The units major features include:

- Multiple sector and track read/write commands
- Host DMA and programmed I/O data transfers
- High performance digital data separation

BIOS (P)ROM/RAM Option

Controller circuitry accommodates a programmed BIOS device for special applications. One unique feature of this BIOS option is its shadow RAM. The static RAM (which shares with the BIOS (P)ROM the last 256 upper address bytes of the BIOS's 8 Kbyte address range) contains the Winchester drive's parameters. This shadow RAM feature allows the WFDC to interface with all types of ESDI drives without modifying the system BIOS. Option jumpers allow the device to be mapped at one of four address ranges. For more information, refer to the jumper configuration tables on page 10 through 13.

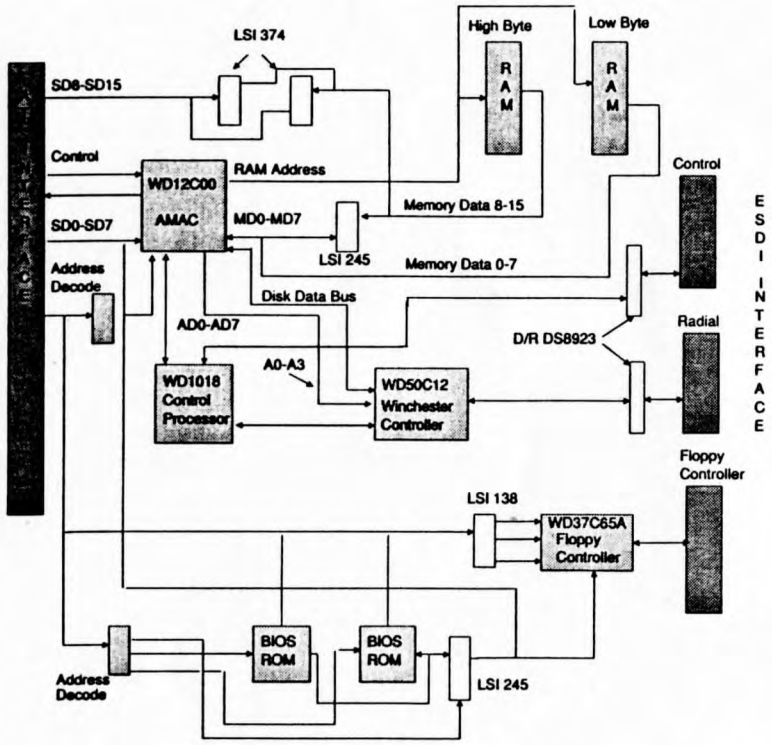

FIGURE 1. WD1007A-WA2 BLOCK DIAGRAM

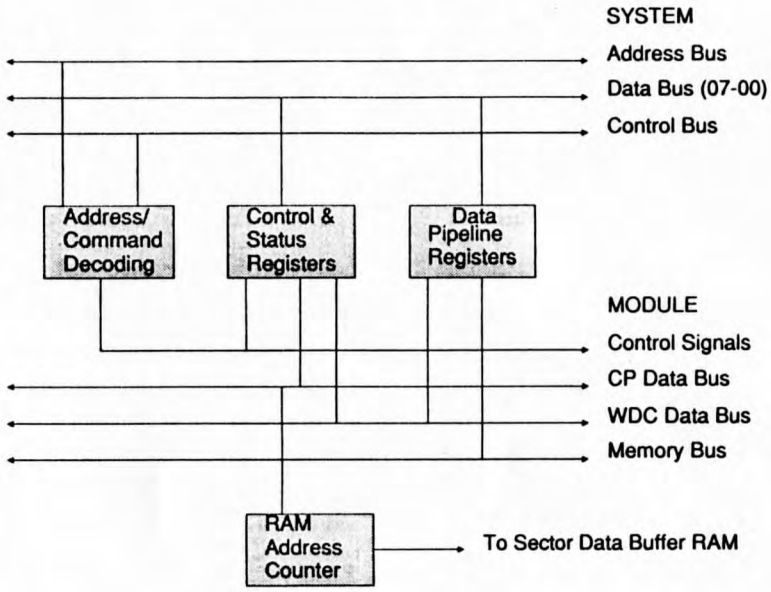

FIGURE 2. AMAC BLOCK DIAGRAM

INTERFACE DESCRIPTION - HARDWARE

System Bus Interface

The WFDC interfaces with the system bus address to transmit data and I/O control signals. All fixed disk read/write data transfers are 16-bits wide and utilize the host I/O transfer protocol. Floppy disk data, fixed disk control, floppy disk control, and status transfers are 8 bits wide and use the lower data byte (SD07-00) only. The register address map of the WFDC module is fixed (at a primary or secondary range) as are the bus interrupt requests and the Floppy DMA channel assignment.

Tables 1 and 2 below provides the pin descriptions for the P1 and P2 system bus connectors.

TABLE 1. SYSTEM INTERFACE CONNECTOR (P1)

PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
A1,A10,B4, B5,B7-B9,B15-B21,B23-B25,B30	NC	Not Connected		
A02-A09	SD07-SD00	System Data Bus	I/O	Transfers 16-bit fixed disk data, 8-bit floppy data and 8-bit module control and status information.
A11	AEN	Address Enable	I	Indicates a valid I/O address is on the system bus. The AMAC decode logic uses this term to qualify the I/O address decoding.
A12-A31	SA19-SA00	System Address Bus	I	Selects the WFDC I/O addresses and BIOS ROM addresses.
B01,B10,B31	GND	Ground		
B02	RST	Reset	I	Input module reset used to initialize the WD50C12, WD1018 and WD37C65A; clear the interrupt levels; and deselect the hard disk drives. When Reset clears, the WD1018 will automatically execute on-board diagnostic tests and load the test result status into the Fixed Disk Error Register.
B03,B29	VCC			
B06	DRQ2	DMA Request Level 2	O	When a data byte is ready for transfer to or from the host memory, the WD37C65A floppy controller generates this signal.
B11	-SMEMW	System Memory Write	I	Input strobe used to write drive parameters in the Shadow RAM.
B12	-SMEMR	System Memory Read	I	Enables BIOS ROM and shadow RAM.

TABLE 1. SYSTEM INTERFACE CONNECTOR (P1) Continued

PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
B13	-IOW	I/O Write	I	Asserted by the system processor during bus 'write' cycles. The WFDC uses this strobe and the decoded bus address to input both data and command information.
B14	-IOR	I/O Read.	I	Asserted by the system processor during bus 'read' cycles. The WFDC uses the signal (along with the system address bus decoding or DMA ACK signal) to enable system I/O reads of both data and command information.
B22	IRQ6	Interrupt Request Level 6.	O	Floppy controller interrupt request to the system processor indicating that the WD37C65A has completed the execution phase of a command or that the selected 'drive ready' line has changed state. Reading the result phase status or issuing a Sense Interrupt Status command will clear the IRQ6.
B26	-DACK2	DMA Acknowledge Level 2.	I	Indicates the completion of a data byte transfer. The DMA controller provides bus control and system memory address.
B27	T/C	DMA Terminal Count	I	The WD37C65A terminates the data transfer sequence for read, write or scan commands when the DMA controller issues this signal.
B28	BALE	Bus Address Latch Enable.	I	Input control signal used to initiate a data transfer on the system bus. The WFDC uses this input to generate the I/O transfer control signal and to enable control signals for high-order data bytes.

TABLE 2. SYSTEM INTERFACE CONNECTORS (P2)

PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
C1-C10,D1, D3-D6, D8-D15,D17	NC	Not Connected		
C18-C11	SD15-SD08	System Data Bus	I/O	Transfers 16-bit fixed disk data, 8-bit floppy data and 8-bit module control and status information.
D02	-I/OCS16	I/O Control Signal 16	O	Indicates 16-bit data transfer mode. The WFDC asserts this signal for all hard disk data transfers.
D07	IRQ14	Interrupt Request Level 14	O	Output to the processor from the fixed disk control requesting a data block transfer or indicating command completion. The level clears on a subsequent fixed disk command to the WFDC or a system reset.
D16	VCC			
D18	GND	Ground		

Winchester Drive Interface

The WFDC module interfaces to the fixed disk drives via one 34-pin control cable (J1) and two 20-pin data cables (J2,J3) in conformance with ESDI signal definitions. The WFDC module does not furnish drive power. Signal descriptions appear in Tables 3 and 4.

TABLE 3. FIXED DISK DRIVE CONTROL CONNECTOR (J1)

PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1,3,5,7,9,11, 13,15,17,19, 21,23,25,27, 29,31,33	GND	Ground		Pin 15 keys the connector.
2,4,18,14	HS3-/0-	Head Select	O	Binary-coded select signals allows selection of drives with up to 16 read/write heads.
6	WRG-	Write Gate	O	Enables the selected drive to accept write data. A write fault condition or a module reset will clear this signal.
8	CSD-	Configuration/ Status Data.	I	Data from the selected drive in response to controller command.
10	TXACK-	Transfer Acknowledge.	I	Handshake response from selected drive acknowledging the controller's transfer request. The drive then accepts command/data or returns configuration/status information.
12	ATN-	Attention	I	Control signal from the selected drive that indicates the drive has a faulty condition or a change of status. This signal is active also during drive power-up sequence.
16	SCT-	Sector Pulse (or Address Mark Found)	I	Sector clock from the selected drive. Used for hard sectored format to mark the beginning of each sector. Used for soft-sectored format to flag detection of an address mark.
20	INDEX-	Index	I	Positioning signal from the drive that occurs once per drive revolution. Used by the WDC for track formatting and command timeout.
22	DRDY-	Drive Ready	I	Control signal from the drive indicating the drive's motor is up to speed and that the I/O control signals are valid.
24	TXREQ-	Transfer Request	O	This control signal sets for command/data information transfers to the drive or for configuration/status information transfers from the drive.
26,28	DS0-, DS1-	Drive Select	O	WFDC selects only Drive 0 or 1.
32	RG-	Read Gate	O	Enables the selected drive to send read data. Controls the drive VCO and data recovery circuit.
34	CMDDAT-	Command Data	O	Sixteen-bit serial data plus parity sent to the selected drive. Data contains instructions for drive execution, i.e., recalibrate, seek, request status.

TABLE 4. FIXED DISK DATA CONNECTORS (J2, J3)

PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
9,20	NU	Not Used		
1	DSLTD 0,1-	Drive Selected	I	Status signal from the drive informing the controller of the selection status after it has asserted a drive selection signal.
3	CMDCPLT 0,1-	Command Completed	I	Status signal from each drive indicating completion of any command.
4	AME 0,1-	Address Mark Enable	O	Control output to each drive used to write address mark onto the disk or search for address mark.
5,6,15,16, 19	GND	Ground		
7,8	WCLOCK 0,1+ WCLOCK 0,1-	Write Data Clock	I	Differential signal for synchronizing write data operations. Derived from reference clock.
10,11	RCLK 0,1+ RCLK 0,1-	Read/Reference Clock	I	Differential signal from the drive used to determine data transfer rate. The drive's data recovery circuits supply the read clock during read data transfers. At all other times the drive furnishes the reference clock.
13,14	WDATA 0,1+ WDATA 0,1-	Write Data	I	Differential write data to be written to each drive.
17,18	RDATA 0,1+ RDATA 0,1-	Read Data	I	Differential read data input from each drive.

Floppy Drive Interface

The controller interfaces to the floppy drives via one 34-pin data and control cable (J4) per the 5.25 inch PC-AT standard. Table 5 below provides the pin descriptions.

TABLE 5. FLOPPY DISK DRIVE INTERFACE (J4)

PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1,3,5,7,9,11, 13,15,17,19, 21,23,25,27, 29,31,33	GND	Ground		Pin 5 keys the connector.
4,6	NC	Not Connected		
2	DRATESLCT	Dual Rate Select	O	Selects either 360 rpm or 300 rpm for dual-speed drives.
8	IDX-	Floppy Index Pulse	I	Positioning signal used by the FDC to indicate the beginning of a disk track.
10	MO1-, M02-	Floppy Drive Motor Enable	O	Signal from the Digital Output Register to enable either drive.
14,12	FDS2-,FDS1-	Floppy Drive Select 1 and 2.	O	Select signals from the FDC operations register. A system master reset or a software reset will inactivate these signals.

TABLE 5. FLOPPY DISK DRIVE INTERFACE (J4) Continued

PIN	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
18	DIRC-	Direction Control	O	Determines the head 'step' direction of a selected drive during controller seek operations. When asserted (low), the step direction is toward the inner tracks.
20	STEP-	Step	O	Step pulses to the selected drive from the FDC. FDC's Specify command controls the rate.
22	FWD-	Floppy Write (MFM or FM)	O	Data input to selected drive.
24	FWE-	Floppy Write Enable 0	O	Enable signal from FDC to selected head.
26	TRK0-	Floppy Track 0	I	During seek operations, the selected drive issues a positioning flag to indicate head position over the outermost track.
28	FWP-	Floppy Write Protect	I	Write protect status from selected drive.
30	FRDD-	Floppy Read Data	I	Output from selected drive.
32	FHS-	Floppy Head Select	O	Head select signal to the active drive. A low signal selects Head 1.
34	DCHG-	Diskette Change Status	I	Used for host control of diagnostic information.

WFDC Configuration

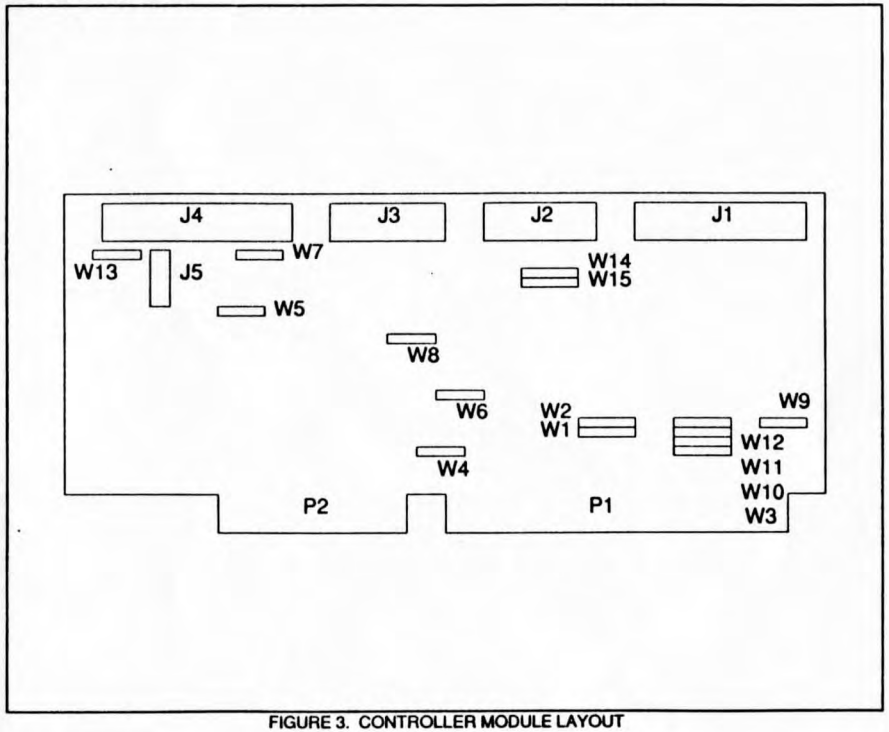

FIGURE 3. CONTROLLER MODULE LAYOUT

Figure 3 illustrates the general module jumper placement and approximate connector locations. The module dimensions are 13.12 by 4.2 inches and a mounting bracket is included. Jumper configurations for the WFDC module appear in Table 6.

Table 6 below lists the default settings for the WD1007A-WA2 which supports two 5.25 or 3.5 inch drives. The WD1007A-WAH is a hard disk only version of the controller.

TABLE 6. JUMPER DEFAULT SETTINGS

JUMPER FUNCTION	WD1007A-WA2		WD1007A-WAH	
BIOS Address Select (C8000-09FFF)	W1	2-3	W1	2-3
BIOS Address Select	W2	2-3	W2	2-3
BIOS Shadow RAM Enabled	W3	Jumper	W3	Jumper
Floppy Controller Enabled	W4	No Jumper		
Single Spindle Speed Selected	W5	No Jumper		
Floppy Address Select (3FX)	W6	2-3		
Floppy Drive Type -	W7	1-2		
WD1007 Mode	W8	No Jumper	W8	No Jumper
Chassis Ground Disconnected	W9	No Jumper	W9	No Jumper
Digital Input Register Unlatched	W10	No Jumper	W10	No Jumper
Diskette Change Enable with FDC Option	W11	Jumper	W11	No Jumper
Secondary Address Select (1FX)	W12	No Jumper	W12	No Jumper
Floppy Controller Enabled - In Etch	W13	Uncut		
Sector Translation Enabled	W14	No Jumper	W14	No Jumper
ECC Length Select (4 Bytes)	W15	No Jumper	W15	No Jumper

Address Select Jumpers

Table 7, Address Select Jumpers, lists the various jumper configurations for address selections for both the hard drive and the floppy drive. Jumper connections W1-W2 select the BIOS ROM/RAM memory addresses. The default address range (C8000 - C9FFF) is factory set. Jumper connection W3 enables the ROM/RAM BIOS when it is jumpered.

Jumper connection W6 selects the floppy drive's address ranges. The default range is 3FX.

The module's primary hard disk address range is (1F0-1F7 and 3F6-3F7). To select the secondary hard disk address range (170-177 and 376-377), jumper the W12 connector.

TABLE 7. ADDRESS SELECT JUMPERS

BIOS ADDRESS RANGES	JUMPER SETTINGS		
	W1	W2	W3
C8000 - 09FFF	2 - 3	2 - 3	Jumper
CA000 - CBFFF	2 - 3	1 - 2	Jumper
CC000 - CDFFF	1 - 2	2 - 3	Jumper
CE000 - CFFFF	1 - 2	1 - 2	Jumper
FLOPPY ADDRESS RANGES	**W6**		
37X	1 - 2		
3FX	2 - 3		
PRIMARY/SECONDARY HARD DISK ADDRESSES	**W12**		
1FX	No Jumper		
17X	Jumper		

Diagnostic Register Latch Control

When installed, jumper connection W10 enables the diagnostic Digital Input Register for operation in the latched mode; i.e., the register outputs latch when the register is accessed. The jumper is normally not used.

WD1018 Mode Control

Jumper connections W8, W14, W15 provide three external mode selects to the control processor.

W8 Jumper Connection

W8 (No Jumper) - This is the normal WD1007A-WAH/WA2 mode. The firmware forces a 10 Mhz ESDI drive to 35 sectors per track when using the Set Unformatted Bytes per Sector command. It is not necessary to set the drive's jumpers and switches for the desired number of sectors per track. This mode supports a 1:1 interleave.

W8 (Jumper) - This mode allows the 1007A-WAH to be used as a replacement board for existing WD1005-WAH boards without reformatting the drive. The controller reads the Unformatted Bytes per Sector from the drive. Consult the WD1007A-WAH/WA2 User's Guide for more information.

W14 Jumper Connection

Because some of the older operating systems can only recognize 17 sectors per track or a maximum of 1048 cylinders per drive, the WD1007A-WA2 provides a translation scheme so that ESDI hard disk drives can be fully utilized in the PC/AT environment.

W14 (No Jumper) - The translation mode provides two types of physical to logical translation. See Translation, page 30 for explanation.

W14 (Jumper) - Physical to logical translation by the firmware is disabled.

W15 Jumper Connection

The purpose of this jumper is to support either four or seven bytes of syndrome during Read or Write Long commands. Four bytes of ECC is the default mode. Installing the jumper provides seven bytes of ECC.

W15 (No Jumper) - 4 Bytes ECC

W15 (Jumper) - 7 Bytes ECC

Floppy Drive and Data Rate Selection Control

W5 Jumper Connection

Jumper connection W5 selects either a single speed or a dual speed drive. A jumper is not normally installed, causing selection to default to a single speed drive and 125 nanoseconds precompensation.

W5 (No Jumper) - Single Speed

W5 (Jumper) - Dual Speed

W7 Jumper Connection

The WD1007A-WA2 supports 5.25 and 3.5 inch floppy disk drives. Install jumper at W7 (1 - 2).

W4 and W13 Jumper Connections

Jumper connectors W4 and W13 enable the floppy drive controller.

	W4	W13 IN ETCH
ENABLE	No Jumper	Uncut
DISABLE	Jumper	Cut

W11 Jumper Connection

Jumper W11 is the disk change input signal, and must be jumpered if floppy drives are installed.

Mounting Bracket Jumper

Jumper connection W9 allows grounding of the module mounting bracket to chassis or logic ground. The jumper is not normally used.

	W9
Chassis ground connected	2-3
Digital ground disconnected	1-2

INTERFACE DESCRIPTION - SOFTWARE

Register Address Map

Table 8 summarizes the WFDC I/O Register Address Map and includes the WD50C12 task file area, the WD37C65A registers and the module auxiliary support registers. It lists the primary address first with the secondary address shown within parentheses.

TABLE 8. REGISTER ADDRESS MAP

ADDRESS (HEX)	REGISTER	FUNCTION
1F0 (170) RW	HDDTR	Hard Disk Data Register (16 bits)
1F1 (171) WO	HDPLO	Gap, ID PLO and Data PLO Lengths
1F1 (171) RO	HDERR	Error Register
1F2 (172) RW	HDSCT	Sector Count
1F3 (173) RW	HDSSN	Starting Sector Number
1F4 (174) RW	HDCLL	Cylinder Number - Low Byte
1F5 (175) RW	HDCLH	Cylinder Number - High Byte
1F6 (176) RW	HDSDH	Sector Size, Drive/Head Select
1F7 (177) WO	HDCMD	Command Register
1F7 (177) RO	HDSTT	Status Register
3F2 (372) WO	FDDOR	Floppy Digital Operations Register
3F4 (374) RO	FDMSR	Floppy Main Status Register (WD37C65A)
3F5 (375) RW	FDDTR	Floppy Data Registers (WD37C65A)
3F6 (376) WO	HDFDR	Fixed Disk (Control) Register
3F6 (376) RO	HDASR	Alternate Status Register
3F7 (377) WO	FDFCR	Floppy Control Register
3F7 (377) RO	HDDIR	Digital Input Register

Task File Registers

Table 9 summarizes the fixed disk Task File Registers (addresses 1F1/171 through 1F7/177) and their bit assignments with respect to the system processor's lower-byte bus terms (SD07-00).

Host access to these registers is always via the register image contained within the AMAC. The WD1018 control processor has access to both the AMAC and WD50C12 register set.

TABLE 9. TASK FILE REGISTERS

	Bit Positions							
REGISTER	7	6	5	4	3	2	1	0
HDPLO	GAP, ID PLO AND DATA PLO LENGTHS							
HDERR	BBD	ECC	0	INF	0	ACD	TK0	DNF
HDSCT	NUMBER OF SECTORS							
HDSSN	STARTING SECTOR NUMBER							
HDCLL	CYLINDER NUMBER LSB							
HDCLH	0	0	0	0	0	CYLINDER NUMBER MSB		
HDSDH	1	SECTOR		DN	HS3	HS2	HS1	HS0
HDCMD	COMMAND							
HDSTT	BSY	RDY	WFT	SKC	DRQ	CRD	CIP	ERR

Note : Bit 7 is the most significant bit.

WFDC Control and Status Registers

Hard Disk Alternate Status Register (HDASR) 3F6/376 (RO)

This register lies within the AMAC array and provides fixed disk status to the system processor. The register contains a 'real time' section (bits 7, 6, 3 and 1) and a 'register' section set by the control processor at sector transfer time (bits 5, 4, 2 and 0).

Bit Positions

7	6	5	4	3	2	1	0
BSY	RDY	WFT	SKC	DRQ	CRD	IDX	ERR

where:

BSY = Controller Busy Flag

RDY = Ready from selected drive

WFT = Write Fault Flag from WD1018

SKC = Seek Complete Flag from WD1018

DRQ = Data Transfer Request Flag

CRD = Corrected Data Flag from WD1018

IDX = Index Pulse from selected drive

ERR = Error Flag from WD1018

The Alternate Status Register reflects the same status as the WD50C12 Status Register, except for bit position 1 which holds the drive index signal instead of the Command in Progress (CIP) flag. The index bit does not latch and thus follows the drive control signal (approximately a 200 microsecond pulse every 16.7 milliseconds).

The Write Fault bit sets for all the ESDI error conditions. The host processor detects a drive's error by issuing the Initiate ESDI command to read the drive's status.

The host processor can interrogate the register at any time without interfering with other control functions. The host status input at this address will not clear the fixed disk interrupt.

Hard Disk Diagnostic Input Register (HDDIR) 3F7/377 (RO)

The fixed disk Diagnostic Input Register reflects the current state of the floppy diskette change flag and the fixed disk Drive Select, Head Select and Drive Write gate signals (complimented form). When the floppy disk option is not installed, bit 7 remains tri-state.

Bit Positions

7	6	5	4	3	2	1	0
DCG	WTG-	HS3-	HS2-	HS1-	HS0-	DS2-	DS1-

where:

DCG = Diskette Change flag

WTG- = Write Gate on

HS3-/0- = Drive Head Select (binary)

DS2-/1- = Drive Select

The WD1018 generates the head select signals which are not transparent as in previous Western Digital Winchester disk controllers. Before the HDASR can be read correctly, the WD1018 requires a "wake-up" in order to update the head select signals.

Hard Disk Auxiliary Control Register (HDFDR) 3F6/376 (WO)

AMAC's Hard Disk Auxiliary Control Register provides programmable controller reset. It also provides enable/disable control of the fixed disk priority interrupt.

Bit Positions

7	6	5	4	3	2	1	0
0	0	0	0	0	RST	IDS	0

where:

RST = Program controlled (master) reset

IDS = Data Transfer Interrupt Disable

NOTE: The software controlled reset bit (RST) will reset the fixed disk logic for as long as the bit is 'on'. RST must be turned on (for a minimum of 10.0 microseconds), then off, to complete the reset function.

The Interrupt Disable control bit does not clear the interrupt level of the disabled state. A pending interrupt will occur when it is re-enabled. A system Master Reset will disable the interrupt.

Fixed Disk Data Registers

The controller reserves the system's I/O address 1F0/170(H) for programmed transfers of input/output data for the fixed disk. All data transactions on the system bus between the controller and the system processor use a 16-bit word. The controller and AMAC array provide read and write data 'pipeline' registers in order for the sector data memory to function as a dual-port memory. These registers (along with the host's upper byte equivalent) allow the WFDC module to perform concurrent host and WDC memory accesses necessary for multi-sector 1:1 interleaving. The AMAC arbitrates simultaneous host and WDC requests and gates the appropriate address counter to external memory.

WD37C65A Floppy Disk Controller Status/Data Registers

The charts below summarize FDC's status and data read/write registers and bit assignments with respect to the system's lower-byte data bus. The main status register (FDMSR) contains the controller's primary status and may be accessed at any time. It indicates drive busy status and facilitates host/controller data transfers. The data register (FDDTR) is actually a register stack that is written during the WD37C65A command phase and read during the result phase.

FDMSR Register Bits

7	6	5	4	3	2	1	0
RQM	DIO	EXM	CB	0	0	D1B	D0B

FDDTR Register Bits

7	6	5	4	3	2	1	0
READ/WRITE DATA							

where:

RQM = Transfer Request To/From Host

DIO = Transfer Direction, '1' is from WD37C65A to Host

EXM = Not DMA Transfer Mode during command execution phase

CB = Read or Write Command in Progress (Busy)

D1B = Drive B in Seek Mode (Busy)

D0B = Drive A in Seek Mode (Busy)

Data Read/Write Register Stack

Tables 10 and 11 illustrate the write stack registers and the read stack registers, respectively. The stack is accessed at the FDDTR register address 3F5 (375).

TABLE 10. WD37C65A WRITE STACK REGISTER

	Bit Positions							
MNEMONIC	7	6	5	4	3	2	1	0
CMD	MT	MF	SK	CMD CODE				
SEL	0	0	0	0	0	HS	0	US0
C	0	CYLINDER NUMBER						
H	0	0	0	0	0	0	0	HA
R	0	0	0	0	SECTOR NUMBER			
N	0	0	0	0	0	0	1	0
EOT	0	0	0	0	TRACK FINAL SECTOR #			
GPL	FORMAT GAP LENGTH							
DTL	1	1	1	1	1	1	1	1
SC	0	0	0	0	SECTORS PER CYLINDER			
D	(FORMAT) DATA FILLER BYTE							
STP	0	0	0	0	0	0	STP	STP
SHT	STEP RATE TIME (SRT)			HEAD UNLOAD TIME (HUT)				
HLD	HEAD LOAD TIME (HLT)							ND
NCN	0	NEW CYLINDER NUMBER						

MT = Multi-track Mode
MF = MFM Data Mode
SK = Skip Deleted Address Mark
US0 = Unit (Drive) Select B
HS = Head Select 1
HA = Head Address 1
STP = 1 = Scan Compare Contiguous Sectors;
2 = Scan Compare Alternate Sectors
ND = Non-DMA Transfer Mode

Note: The MT, MF and SK command bits set to zero for those commands which do not define them. The FDC digital operations register (FDDOR) selects the drive. The unit select bit (US0) is shown for reference only. The HD bit selects the head. The head address bit (HA) identifies the sector.

TABLE 11. WD37C65A READ STACK REGISTER

	Bit Positions							
MNEMONIC	7	6	5	4	3	2	1	0
ST0		IC	SE	EC	NR	HS	0	US0
ST1	EN	0	DE	OR	0	ND	NW	MA
ST2	0	CM	DD	WC	SH	SN	BC	MD
ST3	FT(0)	WP	RY(1)	T0	WP	HS	US1	US0
C	0	CYLINDER NUMBER						
H	0	0	0	0	0	0	0	HA
R	0	0	0	0	SECTOR NUMBER			
N	0	0	0	0	0	0		BYTES
PCN	0	PRESENT CYLINDER NUMBER						

Where:

IC = Interrupt Code = 0 = Normal Command Termination
= 1 = Abnormal (Error) Command Termination
= 2 = Invalid Command
= 3 = Abnormal (Drive Ready Change) Termination
SE = Seek End
EC = Equipment Check
NR = Drive Not Ready
HS = Current Head Address
US0 = Unit Select B
EN = End of Cylinder
DE = Data Error
OR = Overrun Error
ND = No Data Transferred
NW = No Write
MA = Missing Address Mark
CM = Control Mark Found
DD = Data Field Error
WC = Wrong Cylinder
SH = Scan Equal Hit
SN = Scan Not Hit
BC = Bad Cylinder
MD = Missing Data Mark
FT = Drive Fault
WP = Drive Write Protect
RY= Drive Ready
T0 = Track 0 Flag
TS = Drive Two Sided
HD = Drive Head Address
US1/0 = Drive Select Code = 0 Drive A, = 1 = Drive B

Status Register 3 (ST3) contains the status of the selected drive while status registers 0, 1 and 2 contain information on the controller status and command execution. Registers C, H, R and N contain sector identification information following command execution. Register PCN indicates the current cylinder number (head position) following the Sense Interrupt Status command.

Floppy Auxiliary Control Registers

Operations Register (FDDOR) 3F2/372 (WO)

The Operations Register selects the floppy drive, provides drive motor control, enables or disables the floppy interrupt and DMA functions, and provides a WD37C65A software reset command.

Bit Positions

7	6	5	4	3	2	1	
RSV	RSV	MBE	MAE	IDE	RST	RSV	DSB

RSV = Reserved
MBE = Drive B Motor Enable
MAE = Drive A Motor Enable
IDE = Interrupt and DMA Enable
RST = Floppy Section Reset
DSB = Drive B Select

To enable the floppy section operation, RST and IDE must be set.

Floppy Control Register (FDFCR) 3F7/377 (WO)

The Floppy Control Register selects one of four standard read/write data rates as shown below. The 250 Kbps rate is the default state following any reset.

Bit Positions

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

FR1/FR0 = 00 = 500 Kbps (MFM)
= 01 = 300 Kbps (MFM)
= 10 = 250 Kbps (MFM)
= 11 = 125 Kbps (FM)

SPECIFICATIONS

Power Requirements	
+5 VDC	+/- 5.0% 1.200 amperes
Environmental Requirements	
Temperature	
Operating	10° to 50° Celsius
Non-operating	-40° to 60° Celsius
Humidity	
Operating	8% to 85% non-condensing
Non-operating	5% to 95% non-condensing
Shock and Vibration	
Shock	35G/20MS square wave maximum
Vibration	1G/0-600 Hz, dwell not to exceed 30 seconds at any resonance
Altitude	
Operating	0 to 3000 meters maximum
Non-operating	0 to 5000 meters maximum

Fixed Disk Specifications

Data Transfer Format	NRZ
Data Rate	10 MBits per second
Sector format	512 bytes/sector, 35 sectors/track, hard-sectored format
Drives supported	2 maximum
Heads supported	16 maximum
Cylinders supported	2048 maximum
Error Correction Specifications:	
Method	Polynomial division
Degree	56
Forward polynomial	$X^{56} + X^{52} + X^{50} + X^{43} + X^{41} + X^{34} + X^{30} + X^{26} + X^{24} + X^{08} + 1$
Reciprocal polynomial	$X^{56} + X^{48} + X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^{06} + X^{04} + 1$
Record length (r)	519 X 8 bits maximum
Correction span (b)	11 bits
Single burst detection span	r = 519 X 8
With b = 11	32 bits
Double burst detection span	r = 519 X 8
With b = 11	11 bits
Non-detection probability	1.39(E-17), r = 519 X 8, b = 11
Miscorrection probability	5.84(E-11), r = 519 X 8, b = 11

Floppy Disk Recording Specifications

Data Rates (Standard)	500 Kbps (MFM), 250 Kbps (MFM)
	125 Kbps (FM)
Data Rates (Non-standard)	300 Kbps (MFM)
WD37C65A Clocking Rate	500 Kbps (16.0 MHz)
	250 Kbps (16.0 MHz)
	125 Kbps (16.0 MHz)
	300 Kbps (9.6 MHz)
Write Precompensation	125 nanoseconds early/late standard
Sector Format	512 bytes/sector, 15 sectors/track maximum - soft sectored format
Drives supported	2 maximum
Heads supported	2 maximum
Tracks supported	160 maximum
Hard Error Rate	less than 1 per 10(E12) bits read
Soft Error Rate	less than 1 per 10(E09) bits read
Seek Error Rate	less than 1 per 10(E06) seeks

Error Detection/Correction Specifications:

ID Field CRC	$X^{16} + X^{12} + X^{05} + 1$
Data Field CRC	$X^{16} + X^{12} + X^{05} + 1$

Floppy Disk Data Separator Specifications:

Bit Jitter Tolerance	60% (minimum) of window
Capture Range	+/- 8% (minimum)

Timing Specifications

CHARACTERISTIC	MIN	MAX
-IOCS16 from SA09-01		79
-IOCS16 from SA00		38
+IOCS16 from +IOR/+IOW		43
SD15-08 from -IOR		35
SD07-00 from -IOR, Fixed Disk		70
SD07-00 from -IOR, Floppy Disk		90
SD15-08 HIZ from +IOR		43
SD07-00 HIZ from +IOR,Fixed Disk		50
SD07-00 HIZ from +IOR, Floppy		65
SD15-08 setup to +IOW	00	
SD07-00 setup to +IOW,Fixed Disk	30	
D07-00 setup to +IOW, Floppy	80	
+IOW to SD15-08 HIZ (hold time)	25	
+IOW to SD07-00 HIZ (hold time)	20	
-IOR/-IOW pulse width(16 bit I/O)	70*	
-IOR/-IOW pulse width (8 bit I/O)	70*	
+IOR/+IOW to -IOR/-IOW(16 bit I/O	375**	
-DACK2 to -DRQ2	140	
DRQ2 period	3. 2 µsec	
TC pulse width	60	

Note: All timing is in nanoseconds unless otherwise specified.
* Does not include host read data setup time
** 10 MHZ clock input

The I/O address lines (SA09-00) and the address control signal (AEN) connect to the address decode PAL for module selection. Lines SA9 and SA2-0 connect to the AMAC for individual register addressing. The low order data byte (SD07-00) connects directly to the AMAC, and the device provides the necessary bus drive current. Figure 4 illustrates the I/O read and write signal relationship.

AMAC's data pipeline registers allow the WFDC module to perform concurrent host and WDC memory accesses necessary for multisector 1:1 interleaving. A clocked sequencer controls the timing of the two AMAC generated strobes to resolve priority (in favor of the host request) and generate the external memory (and byte transfer gate) control signals.

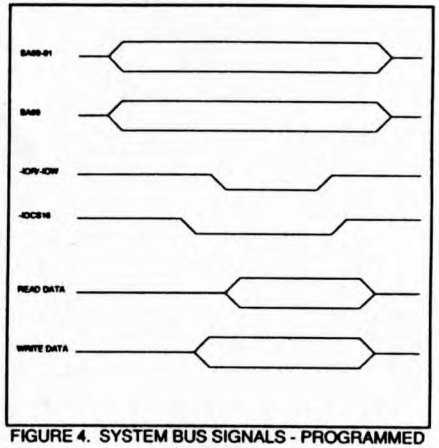

FIGURE 4. SYSTEM BUS SIGNALS - PROGRAMMED I/O CONTROL

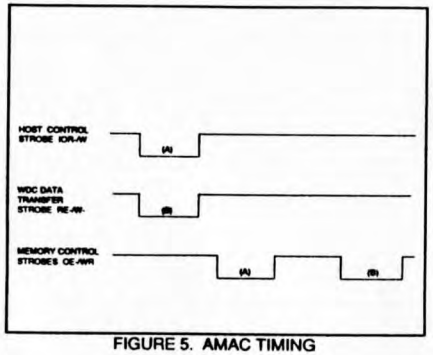

FIGURE 5. AMAC TIMING

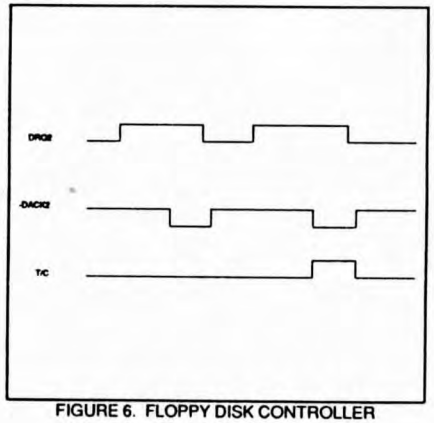

FIGURE 6. FLOPPY DISK CONTROLLER

COMMAND SUMMARY

Software Overview

All control and data transfers between the system processor and the WFDC fixed disk control section use system programmed I/O. Direct memory accesses (DMA) are used in the floppy disk section for data transfers only. All floppy control and status transactions use system programmed I/O. The module address range is fixed (at either of two ranges) as are the controller priority interrupt levels and the DMA channel assignment.

WD50C12 Winchester Disk Controller

Command Code Summary

The Task File Command Register (HDCMD) accepts the commands and command attributes as shown in Table 12. It does not accept commands when the WFDC is 'busy'. Commands terminate without execution if the Drive Ready signal is false, if a write fault condition exists at the drive, or if the command is undefined.

TABLE 12. WD50C12 COMMAND CODE SUMMARY

	Bit Positions							
COMMAND	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RESTORE	0	0	0	1	X	X	X	X
SEEK	0	1	1	1	X	X	X	X
RD SECTOR	0	0	1	0	0	0	LNG	RTY
WRT SECTOR	0	0	1	1	0	0	LNG	RTY
FMAT TRACK	0	1	0	1	0	0	0	0
RD VERIFY	0	1	0	0	0	0	0	RTY
DIAGNOSE	1	0	0	1	0	0	0	0
SET PARAM	1	0	0	1	0	0	0	1
INIT ESDI	1	1	1	0	0	0	0	0
WRT STACK	1	1	1	0	1	0	0	0
RD STACK	1	1	1	0	0	1	0	0
READ PARAM	1	1	1	0	1	1	0	0
CACHE CNTL	1	1	1	0	1	1	1	1

Where:

X = Drive stepping rate. (Unused in ESDI drive)

LNG = 0 = Normal mode, WD50C12 performs normal ECC functions.

LNG = 1 = Long mode, the WD50C12 is unable to generate or check the ECC bytes. The WD50C12 appends the additional bytes supplied by the drive (read) or host processor (write) to the normal data field.

RTY = 0 = Error retries and ECC correction are enabled

RTY = 1 = Retries and ECC correction are disabled.

Standard AT Commands

The WD50C12 executes the following standard commands:

Command	Op Code
Read Sector	20H
Write Sector	30H
Restore	1XH
Set Parameters	91H
Format Track	50H
Diagnose	90H
Seek	7XH
Read Verify	40H

Scan ID and Compute (ECC) Correction commands are not directly available to the system processor (although they may be executed by the WD1018 transparently to the host processor).

Read Sector - A number of sectors (1-256) are read from the selected disk. If the drive is not positioned at the specified cylinder an implied 'seek' will occur. Drive furnished ECC check bits will be used if the Read Long mode is specified. Single burst data errors (up to 11 bits) will be corrected if retries are enabled and the long mode is not selected.

Uncorrectable errors do not inhibit the (error sector) data transfer, however, multi-sector transfers will terminate. The WFDC interrupt occurs as each sector is ready for system input. The WFDC also caches the remaining sectors until the buffer RAMs are full upon completion of a successful Read Command. When the next Read Command occurs, and if the desired sectors are the same as the cached sectors, the data transfer occurs immediately. Caching therefore improves the data throughput by reducing the disk access time. IRQ14, BSY and DRQ bits of HDSTT register operate in the same fashion as in non-cache operations.

Write Sector - A number of sectors (1-256) are written to the selected disk with an implied seek occurring, if required. Multiple sector write (and read) operations may cross track and cylinder boundaries. The Write Long mode appends the ECC bytes to the data supplied by the system processor. The data request bit (On) along with the command cause the system processor to output the contents of the first data buffer. An interrupt occurs as the data for each subsequent sector is required.

Restore - The selected ESDI drive receives a Seek-to-Cylinder 0 command via the serial command interface (WD1018 port 1.5). The drive heads seek to cylinder 0 and any track offsets are clear. The command aborts when the ERR bit sets in the status register. The Aborted Command (ACD) bit sets in the error register if the WD1018 receives an Attention interrupt from the drive indicating a transfer protocol or transfer parity error.

Set (Drive) Parameters - This command communicates drive parameters to the controller. It selects the head, cylinder, and sector for each drive. The WD1018 uses the drive parameters in the execution of multi-sector commands and in evaluating legal controller commands.

Format Track - The Task File specifies the track to be formatted with identification, data, and check fields in accordance with the interleave table transferred to the sector buffer. The interleave table is composed of two bytes per sector, with the first byte set to "00" for a good sector or "80h" for a bad sector. The second byte designates the logical sector number. The Task File (HDSCT and HDSDH) specifies sectors per track and sector size. Command completion initializes the data field to 'zeros' and appends four ECC bytes after the data field. The Completion Interrupt occurs as each track is formatted. The WD1007A-WA2 controller forces 512 bytes/sector, 35 sectors/track, and the hard sectored drive format.

Diagnose - The diagnostic command causes the WD1018 to execute an on-board diagnostic program and to report the test results to the WD50C12 Error Register. See Appendix for WFDC self tests.

Seek - The Seek command positions the drive heads over the cylinder specified in the Task File registers (HDCLH/L) and clears any track offsets. The command aborts under the conditions noted for the Restore command above. Bit SKC of the HDSTT register sets true upon the completion of a Seek command. The fixed disk priority interrupt (IRQ14) issues after a successful ESDI Seek command transfer. The host can check for completion of the seek operation by checking bit SKC of HDSTT register.

Read Verify - This command verifies that a previous write command is correct by checking ECC bytes. The host processor does not input read data. The command may be used with multi-sector operations. An error condition will abort a

multi-sector verify operation. The retry command may be used with this command.

Non-standard AT Commands

The WD1018 intercepts fixed disk commands to the WFDC with the aid of the AMAC logic in order to define commands not specified in the WD50C12 command list.

Command	Op Code
Write Data Stack	E8H
Cache Control	EFH
Read Parameters	ECH
Read Data Stack	E4H
Initiate ESDI	EOH

Write Stack - This diagnostic command allows the host to write data to the sector buffer without executing an actual disk write command. This command does not generate an interrupt upon completion.

Cache Control - This command (EF) allows the user to enable or disable caching. By writing AA (enable) or 55 (disable) into the Write Precomp Register (1F1), then issuing the Cache Control command, caching will be turned on or off accordingly. The command will abort if any another code is written into 1F1, and caching stays unchanged. Caching is enabled in default.

When cache control is enabled, the WFDC reads ahead and buffers data sectors that are likely to be requested by the host on subsequent read commands. When executing a read command, the WFDC reads ahead until the buffer RAM is full. When the next read command occurs, the data transfer will occur immediately if the desired sectors are within the cached sectors. Caching starts with the next sector after the sector specified by the host command. A sector with a number lower than the specified sector is not cached. The WFDC continues to cache when reading across tracks, but will empy out the buffer when reading across heads or when changing from a read to a write command.

Read Parameters - This command causes the WD1018 to store 49 words of drive and controller parameters into the sector buffer for host access. The data is stored in the format shown in Table 13.

Read Stack - This diagnostic command allows the host to read the sector buffer without executing a disk read operation. This command does not generate an interrupt upon completion.

Initiate ESDI - This command allows the system processor to send instructions directly to the selected drive by loading the AMAC's cylinder register and executing the Initiate command. The host must load AMAC's cylinder registers (high and low data bytes) with the command it wants the drive to execute prior to issuing the Initiate ESDI command. The controller serializes the data, adds the required parity bit and transmits the instruction to the drive. The drive completes the instruction and transmits completion status to the controller. The drive's completion status data is then stored back into AMAC's cylinder registers for host access.

The high byte (bits 15 - 8) of the ESDI command goes to Cylinder High Register, and the low byte (bits 7 - 0), if applicable, goes to Cylinder Low Register. Refer to ANSI ESDI Specification, Document No. X3T9.3/8X, for all ESDI commands.

The host can now access the drive's status by reading the cylinder register's addresses (AF4 - AF5).

Using DEBUG, enter:

```
O1F4 00
O1F5 20; Output Read Status Command
O1F7 E0; Initiate ESDI Command
I1F4
I1F5; Read Drive Status
```

Multi-sector Commands

The WFDC provides multiple sector read, write and verify commands of up to 256 sectors without restriction on track or cylinder boundaries. Unrecoverable control errors (Drive Not Ready, Write Fault, etc.) or uncorrectable read data errors will terminate a multi-sector command, and the controller expects a new command to continue operation. Corrected read data errors do not terminate the command, and the controller expects a normal data transfer restart and continuation. WFDC can execute 'long mode' ECC diagnostic commands, however, the throughput is reduced.

Diagnostic Commands

The controller on-board diagnostic verifies the WD1018 local storage, the sector data buffer storage and the data paths for WD1018, WD50C12 and AMAC. The encoded results are available to the system processor via the controller error register.

TABLE 13. READ PARAMETERS

OFFSET	MODIFIER Bits 8 - 11	ESDI CONFIGURATION INFORMATION
0	0	General Configuration
1	1	Number of fixed cylinders
2	2	Number of removable cylinders
3	3	Number of heads
4	4	Number of unformatted bytes per track
5	5	Number of unformatted bytes per sector
6	6	Number of sectors per track
7	7	Number of minimum bytes in ISG
8	8	Number of minimum bytes in PLO
9	9	Number of words of vendor status
OFFSET		**CONTROLLER PARAMETERS**
10 - 19	Serial # (20 ASCII characters - 0)= not specified)	
20	Controller type 0= not specified 1= single port, single sector buffer 2= dual port, multi-sector buffer 3= dual port, multi-sector buffer, cache	
21	Controller buffer size in 512 byte increments (32 sectors)	
22	Number of ECC bytes transferred on long operations (4 ECC bytes)	
23 - 26	Controller firmware revision (8 ASCII characters)	
27 - 46	Controller model # (40 ASCII characters)	
47	Number of sectors transferred per INT on read commands (1 sector/interrupt)	
48	Double word capability 0= not capable 1= capable	

WD37C65A Floppy Disk Controller

Standard AT Commands

The WD37C65A executes the following standard commands: Read Data, Read Deleted Data, Write Data, Write Deleted Data, Read Track, Read ID, Format Track, Scan (Data) Equal, Scan Low or Equal, Scan High or Equal, Recalibrate, Sense Interrupt Status, Specify, Sense Drive Status and Seek.

The WD37C65A has a specific command, execution and result phase protocol for each command. The floppy disk section commands are listed below along with their respective command codes, command phase (write) register stack and result phase (read) register stack.

Read Data - The host outputs the nine command phase bytes and the FDC selects the drive, loads the drive heads (if previously unloaded) and begins reading ID address marks and ID data fields to locate the selected sector. When the sector is found the FDC transfers data (via DMA) to host memory. Multi-sector and multi-track operations are allowed. Completion of the command updates the result phase registers, interrupts the system processor (if interrupt enabled) and unloads the heads following the head unload interval.

The **Read Deleted Data** command and **Read a Track** command have the same command and result phase register requirements except for the command opcode. The Read Deleted Data command transfers sectors which have the deleted data address mark. The Read Track command transfers all sectors from the index mark through the 'end of track' sector.

A **Read Identification Field** command transfers the first correct ID field data to the sector identification result registers and interrupts the host. Sector data does not transfer to system memory. The result register stack is the same as for a normal read command but the command phase requires only the command and select register information.

Write Data - The host outputs the nine command phase bytes and the FDC selects the drive, loads the heads and searches the sector ID fields. When the C, H, R and N sector fields match the command register data the FDC transfers byte data via DMA to the drive. Command completion updates the result registers and interrupts the host processor.

The **Write Deleted Data** command is the same as Write Data except that a deleted data address mark appears at the beginning of the data field in place of a normal data address mark.

Format a Track - The FDC formats the selected track from index through the last track sector with address marks, ID fields, data fields and field gaps for either the single or double density format. The host furnishes the ID field data (four bytes) for each sector. The data field is filled with the data defined in the Command Stack Register D.

Scan Equal - The FDC compares the drive information and the host data for a selected sector on a byte basis. If the scan condition is satisfied, the SH (scan equal hit) bit sets in Status Register 2.

The **Scan Low or Equal** and **Scan High or Equal** commands are similar except for the logical compare condition. If the scan condition is not satisfied, the SN (scan not hit) bit sets in Result Register ST2.

Recalibrate - The heads of the selected drive retract to track position 0. The track 0 position flag is available as a separate signal from the selected drive and in the ST3 status byte.

Seek - The selected drive steps to the new cylinder position.

Specify - The Specify command sets the drive head's load and unload rates, the drive's step rate, and the DMA data transfer mode.

Sense Interrupt Status - Controller status register 0 and the current cylinder are available in the result registers following this command. This command clears the floppy section's interrupt level.

Sense Drive Status - This command returns selected drive status (ST3) during the result phase.

Non-standard Commands

The WD37C65A has two registers in addition to the industry standard UPD765 registers. They are: the Operations Register which controls the floppy drive select, drive motor enables, controller reset, DMA request, and interrupt enable; and the Control Register which selects the floppy data rate.

WD1018 Commands

The WD1018 communicates with the AMAC support logic via a set of read/write commands at preset addresses. The commands are avail-

able to the controller only and not to the system processor. (See Table 14)

TABLE 14. CENTRAL PROCESSOR SUPPORT COMMANDS

ADDRESS	R/W	COMMAND
20	R/W	Host memory address block counter
21	R/W	WDC memory address block counter
22	W	Clear host memory address counter
22	R	Set sleep mode (clear busy)
23	W	Clear WDC memory address counter
23	R	Set 7 byte ECC mode
24	W	Set data request latch
24	R	Set interrupt
25	W	Set read mode
25	R	Set memory prefetch
26	W	Set multiple sector mode
26	R	Clear multiple sector mode
27	W	Set sector block counter
27	R	Set idle mode

Addresses 00-07(H) and 10-17(H) are reserved for CP communication with the AMAC and WD50C12 Task File registers respectively. Address range 30-3F(H) is reserved for special IDE and command control.

NOTE: The two high order address bits are not used in the AMAC address decode of the WD1018 support commands.

APPENDIX

WFDC SELF TESTS

The encoded result descriptors for each controller self test are shown in Table A-1. The WFDC error register HDERR (hex address 1F1/171) reports the test result. Issuing a Diagnose command or a reset will execute the tests.

The tests verify the WD1018 firmware checksum, the WD1018 RAM memory, the sector buffer RAM memory and the WD50C12 and AMAC data paths. System bus or host interactive tests are not included.

RESULT	DESCRIPTION
01	No Errors
02	Controller Error
03	Sector Buffer Error
04	AMAC Device Error
05	Control Processor Error
06-FF	Undefined

where:

02 = WD1018/WD50C12 register access error

03 = Sector buffer data error

04 = WD1018/AMAC register access error

= AMAC Byte 0 Pipeline register error

05 = WD1018 ROM checksum error

= WD1018 RAM data error

1007A-WA2 OPTIONAL BIOS

General

The WD1007A controllers have an optional BIOS ROM that enables the user to integrate a controller having an ESDI drive with an IBM PC/AT or compatible. The BIOS provides drive parameter tables, low-level formatting routines, and surface analysis routines. The parameter tables support the drive and controller in systems that do not provide ESDI parameters. Low-level formatting and verification routines prepare the drive for use by the operating system. Part of the optional BIOS is a "shadow RAM". This is a static memory device that resides in the upper 256 bytes of the BIOS address space. This memory stores the parameter information generated by the BIOS in an area outside system memory. The BIOS resides in the external I/O BIOS address space. There are four address ranges available, which are selected by configuring the jumpers at W1-W2. (Refer to the Jumper Configuration Tables, page 11.)

Parameter Tables

Most system BIOS ROMS support only the older MFM/ST-506 drives that used 17 sectors per track. The ESDI disk drive typically has 34 sectors per track when operating in the hard sector mode. The BIOS generates the needed information by using the ability of the ESDI drive to present the actual drive characteristics to the controller. The BIOS reads the ESDI information and generates the appropriate parameter tables. Parameter tables are also constructed for the translation features of the controller.

Format and Surface Analysis

Formatting routines perform the low-level initialization of the disk surface. The drive is formatted with the physical characteristics read from the drive. Formatting is done at a 1:1 interleave ratio and is not changeable. The format routine formats with a sector skew and also formats a spare sector on each track. This sector is used by the surface analysis routines to provide the ability to reallocate a bad sector on a track. It also stores the parameter information generated by the BIOS. This information appears on the spare sector on cylinder 0, head 0. The sector skew which is fixed at two, allows the controller to maintain a 1:1 interleave across all head boundaries. Sector skewing is a method of formatting in which the sector numbers are rotated in the interleave table for each track. Refer to the WD1007A-WAH/WA2 Application Notes for a more detailed description of the BIOS and its use.

Translation

MS-DOS assumes that a hard disk has 17 sectors per track (SPT). This reflects the ST-506 type drives. However, the ESDI drives support 34 to 36 sectors per track with 512 bytes per track. In order to utilize the maximum storage capacity of the ESDI drives, the WD1007A-WA2 controller provides two methods of translation:

1. Translation of 17 sectors per track mode

For those operating systems that recognize only 17 sectors per track, it is necessary to translate physical sectors per track into logical sectors per

track. This is accomplished by setting the number of logical heads requested in the SDH register to twice the number of physical heads (for a maximum of 16 heads). This mode is invoked when the host issues a Set Parameters command with 17 in the Sector Count Register.

The WD1007A-WA2 utilizes the 35 physical sectors by designating either sector 0 or 35 as the optional alternate sector and dividing the remaining 34 sectors between two logical heads. For example, if sector 0 is the alternate sector, then sectors 1 through 17 represent a logical track or logical head 0. Sectors 18 through 34 represent a logical track or logical head 1.

PHYSICAL PARAMETERS	LOGICAL PARAMETERS
1024 Cylinders	1024 Cylinders
8 Heads	16 Heads
34 Sectors per Track	17 Sectors per Track

Low-level formatting of ESDI drives must be accomplished with 0-34 or 1-35 sectors per track. If a format for 17 sectors per track is attempted, only the data fields will be initialized.

2. General translation mode

This mode is invoked when the physical number of cylinders exceeds 1024. By increasing the logical sectors per track to 63 and increasing the logical heads to 16, the number of logical cylinders will decrease accordingly.

For this type of drive, the following algorithm for disk address translation is used:

*ABS_SEC = (((LOG_CYL * LOG_HDS) + LOG_HD) * LOG_SPT) + LOG_SEC -1*

ABS_HEAD = ABS_SEC DIV PHY_SPT

PHY_SEC = ABS_SEC MOD PHY_SPT + 1

PHY_HEAD = ABS_HEAD MOD PHY_HEADS

PHY_CYL = ABS_SEC DIV PHY_HEADS

Where :

ABS_SEC is the absolute logical sector number with range 1 through 1,032,192.

LOG_HDS is the maximum number of logical heads 1 - 16

LOG_SPT is the logical sector/track 1 - 63

LOG_SEC is the logical sector address 1 - 63

LOG_HD is the logical head address 0 - 15

LOG_CYL is the logical cylinder address 0 - 1023

PHY_HEADS is the maximum number of physical heads

PHY_SPT is the disk sector/track = 34

PHY_SEC is the disk physical sector 1 - 34

PHY_HEAD is the disk physical head 0 - 15

ABS_HEAD is the calculated absolute head address 0 - 19114

PHY_CYL is the disk physical cylinder address

Physical to Logical Formulas:

*ABS_SEC = (((PHY-CYL * PHY_HEADS) + PHY_HEAD)*PHY_SPT)+PHY_SEC*

LOG_SEC = ABS_SEC MOD LOG_SPT

ABS_HEAD = ABS_SEC DIV LOG_SPT

LOG_HEAD = ABS_HEAD MOD LOG_HEADS

LOG_CYL = ABS_HEAD DIV LOG_HEADS

Translation Algorithm Example:

The following translation example uses an HP 9753XEA ESDI.

HP 9753XEA physical parameters:

PHY_CYLS = 1600 Cylinders

PHY_HEADS = 12 Heads

PHY_SPT = 32 sectors per track (actually 64,256 byte sectors)

By transposing these values into the following formula, this drive can offer 614,400 sectors:

*ABS_SECS = PHY_CYLS * PHY_HEADS * PHY_SPT*

*ABS_SECS = 1600 * 12 * 32 = 614,400*

The following formula determines the logical parameters:

*ABS_SECS = LOG_CYLS * LOG_HEADS * LOG_SPT*

If the logical sectors per track (LOG_SPT) is 63 and the logical number of heads (LOG_HEADS) is 16, then to determine the logical number of cylinders (LOG_CYLS):

*LOG_CYLS = ABS_SECS / (LOG_HEADS * LOG_SPT)*

*LOG_CYLS = 614,400 / (16 * 63) = 609*

The resulting logical parameter table for the HP 9753XEA would be:

LOG_CYCLS = 609 cylinders

LOG_HEADS = 16 heads

Log_SPT = 63 sectors per track (512 byte sector)

This yields a 314.3 Mbyte drive. The drive would actually have a capacity of 314.5 Mbytes if it could be accessed physically. Only read and write data operations use these logical parameters.

Low level initialization and alternate sector utilization must be accomplished physically. When using diagnostics, such as IBM ADVANCED DIAGNOSTICS, and a format track command issues with a sector count not equal to the physical sectors per track, determine the starting physical sector and write a pattern of zeros in the data field of all sectors on the logical track.